**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**
**(Attorney Docket No. 13912US04)**

In the Application of:

Ichiro Fujimori

***Electronically Filed on 27-APR-2007***

Serial No. 10/801,260

Filed: March 15, 2004

For: SYSTEM AND METHOD TO REDUCE NOISE IN A SUBSTRATE

Examiner: Phat X. Cao

Group Art Unit: 2814

Confirmation No. 2251

## APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from an Office Action dated November 28, 2006 ("Final Office Action"), in which claims 1-15 were finally rejected. The Applicant respectfully requests that the Board of Patent Appeals and Interferences ("Board") reverses the final rejection of claims 1-15 of the present application. **The Applicant notes that this Appeal Brief is timely filed within the period for reply that ends on April 27, 2007.**

## REAL PARTY IN INTEREST
## (37 C.F.R. § 41.37(c)(1)(i))

Broadcom Corporation, a corporation organized under the laws of the state of California, and having a place of business at 5300 California Avenue, Irvine, California 92617, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment recorded at Reel 013786, Frame 0440 in the PTO Assignment Search room.

## RELATED APPEALS AND INTERFERENCES
## (37 C.F.R. § 41.37(c)(1)(ii))

Not applicable.

## STATUS OF THE CLAIMS
## (37 C.F.R. § 41.37(c)(1)(iii))

Claims 1-15 were finally rejected. Pending claims 1-15 are the subject of this appeal.

Claims 1, 8-9, 12 and 14-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,356,497, issued to Puar et al. (hereinafter, Puar), in view of U.S. Patent No. 6,395,591, issued to McCormack et al. (hereinafter,

McCormack).[1] Claims 1-10, 12 and 14-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McCormack in view of Puar.[2] Claims 11 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McCormack and Puar as applied to claim 1, and further in view of U.S. Patent No. 6,403,992, issued to Wei (hereinafter, Wei).[3] Claims 1-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wei in view of Puar.[4] The Applicant identifies claims 1-15 as the claims that are being appealed. The text of the pending claims is provided in the Claims Appendix.

## STATUS OF AMENDMENTS
## (37 C.F.R. § 41.37(c)(1)(iv))

The Applicant has not amended any claims subsequent to the final rejection of claims 1-15 mailed on November 28, 2006.

## SUMMARY OF CLAIMED SUBJECT MATTER
## (37 C.F.R. § 41.37(c)(1)(v))

The invention of claim 1 is illustratively described in the Specification of the present application in, for example, "Brief Summary of the Invention" section in page 4. Certain embodiments of the invention may be found in, for example, a system that

[1] *See* Final Office Action at page 2.
[2] *See id.* at page 3.
[3] *See id.* at page 4.
[4] *See id.* at page 5.

reduces noise in a substrate of a chip[5]. Aspects of the system may comprise a substrate layer (70) that is integrated within the chip and a transistor layer that is integrated within the chip and is shielded from the substrate layer by a shielding layer (80)[6]. At least one transistor of a first transistor type couples the transistor layer to the shielding layer and a quiet voltage source may be coupled to the transistor of the first transistor type[7]. At least one transistor of a second transistor type is coupled to the shielding layer[8].

Claims 2-15 are dependent upon claim 1.

## GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. § 41.37(c)(1)(vi))

Claims 1, 8-9, 12 and 14-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,356,497, issued to Puar et al. (hereinafter, Puar), in view of U.S. Patent No. 6,395,591, issued to McCormack et al. (hereinafter, McCormack). Claims 1-10, 12 and 14-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McCormack in view of Puar. Claims 11 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McCormack and Puar as applied to claim 1, and further in view of U.S. Patent No. 6,403,992, issued to Wei (hereinafter,

[5] *See* the present application at page 4, lines 2-3 and Figure 2.
[6] *See id.* at page 4, lines 3-5 and Figure 2.
[7] *See id.* at page 4, lines 5-7.
[8] *See id.* at page 4, line 8.

Wei). Claims 1-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wei in view of Puar.

## ARGUMENT
## (37 C.F.R. § 41.37(c)(1)(vii))

Claims 1, 8-9, 12 and 14-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,356,497, issued to Puar et al. (hereinafter, Puar), in view of U.S. Patent No. 6,395,591, issued to McCormack et al. (hereinafter, McCormack). Claims 1-10, 12 and 14-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McCormack in view of Puar. Claims 11 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McCormack and Puar as applied to claim 1, and further in view of U.S. Patent No. 6,403,992, issued to Wei (hereinafter, Wei). Claims 1-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wei in view of Puar. The Applicant respectfully traverses these rejections at least for the reasons previously set forth during prosecution and at least based on the following remarks. The combination of Puar, McCormack and Wei, however, does not describe, teach or suggest every recited limitation within these claims. The burden of establishing a *prima facie* case of obviousness resides with the Patent and Trademark Office.[9] The Final Office Action fails to establish a *prima facie* case of obviousness because it does not specifically point to every limitation of the rejected claims of the present application in Puar, McCormack and Wei.

[9] *See* In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984) quoting In re Warner, 379 F.2d 1011, 1016, 154 USPQ 173, 177 (CCPA 1967).

## I. The Proposed Combination of Puar and McCormack Does Not Render Claims 1-10, 12 and 14-15 Unpatentable (Pages 2-4 of the Final Office Action)

The Applicant turns to the rejection of claims 1, 8-9, 12, and 14-15 as being unpatentable over McCormack in view Puar, and claims 1-10, 12 and 14-15 as being unpatentable over Puar in view of McCormack. Since claim 1 is the only independent claim and it is being rejected as unpatentable over the combination of Puar-McCormack (and McCormack-Puar), the Applicant will initially discuss the rejection of claim 1 under 35 U.S.C. § 103(a)

### A. Rejection of Claim 1

With regard to the rejection of independent claim 1 under 103(a), the Applicant submits that the combination of Puar and McCormack (or McCormack-Puar) does not disclose or suggest at least the limitation of "a shielding layer, wherein said shielding layer reduces transfer of noise in the chip," as recited by the Applicant in independent claim 1. The Final Office Action states:

> Puar (Fig. 5) discloses a system for reducing noise in a chip, the system comprising: a substrate layer (P substrate) integrated within the chip; a transistor well layer (N-Well) integrated within the chip; at least one transistor of a first transistor type (P-type) formed within the well layer; and a positive potential of a quiet voltage source Vdd (column 4, lines 59-63) that is coupled to the at least one transistor of the first transistor type.
>
> **Puar does not disclose that the transistor well layer (N-Well) is shielded by a shielding layer.**
>
> However, McCormack (Fig. 2) teaches the forming of a transistor within a transistor well layer and on a lightly doped (p-) substrate layer 50. The transistor well layer is isolated or shielded from the substrate 50 by a p type epitaxy layer 12 disposed therebetween. **The layer 12 functions as a shielding layer for reducing the noise in the chip because it**

> **isolates the substrate 10 from the transistor layer and has a higher doping than the underlying substrate 10 for providing immunity against parasitic substrate effects or latchup effects (column 1, lines 19-24 and column 4, lines 9-13).** Accordingly , it would have been obvious to modify the device of Puar by forming the shielding layer between the substrate layer and the transistor well layer because such forming of the low resistivity shielding layer would isolate the noise transfer to the transistor layer by reducing parasitic substrate effects or latchup effects. (emphasis added)

*See* the Final Office Action at pages 2-3. The Applicant submits that the above bolded statement by the Examiner, namely that **"layer 12 ... has a higher doping than the underlying substrate 10 for providing immunity against parasitic substrate effects or latchup effects"** is completely erroneous and is not supported by McCormack. The Examiner seeks support in column 1, lines 19-24 and column 4, lines 9-13 of McCormack.

McCormack states the following at col. 1, lines 19-24:

> While a lightly doped p-type substrate having a resistivity of 5 or 20 ohm-cm has been used in early fabrication processes, this was found to be problematic for CMOS integrated circuits because the high substrate resistance renders the integrated circuit more susceptible to latchup.

First of all, this citation of McCormack does not relate to any elements disclosed by McCormack. The Applicant is confused as to why the Examiner is citing from column 1, lines 19-24 and column 4, lines 9-13 of McCormack without any support whatsoever that any of the cited material relates to layer 10, layer 12 or, for that matter, to any other element of the invention of McCormack.

McCormack states the following at col. 4, lines 9-13:

> A conventional way to reduce latchup susceptibility is to lower the resistance of the P-wells. A low P-well resistance has the effect of decoupling the parasitic bipolar transistors formed by the source/drain regions and the n and p tubs in a CMOS process.

The Applicant is, again, confused as to why the Examiner is citing col. 4, lines 9-13 as this citation of McCormack relates to the resistance of the p-wells and it does not relate in any way to the doping of layers 10 or 12.

Therefore, **the McCormack reference does not disclose or suggest that the p type layer 12 has higher doping than the lightly doped (p-) substrate 10. In fact, McCormack teaches away from the notion that layer 12 has higher doping than layer 10 as McCormick discloses that the resistance for both the p-type substrate 10 and the p-type epi-layer 12 are in the same 14-28 ohm-cm range.** *See* McCormack, col. 5, lines 45-47 and col. 6, lines 1-3. **Even though McCormack does not disclose specific values for the resistances of substrate 10 and layer 12, within the 14-28 ohm-cm range, the fact that McCormack discloses that the p-type substrate 10 and the p-type epi-layer 12 have resistances in the same range is indicative that McCormack teaches away from the notion that the layer 12 has higher doping than the substrate 10.**

Furthermore, nowhere in the McCormack reference is there any claim or inference that the p-type epitaxy layer 12 functions as a "shielding layer." McCormack **credits the enhanced circuit performance while offering protections against parasitic effects to the heavily doped p++ region 14, not to the p type epitaxial layer 12.** McCormack discloses a selective substrate implant process that "is capable

of enhancing the circuit performance while offering protections against parasitic effects" (Column 2, Lines 57-59) by forming "a heavily doped p++ region 14," (Column 2, Lines 65-66) that is "formed only in areas where P-wells are to be built." (Column 6, Lines 43-44). **Even if the heavily doped p++ region 14 in McCormack functions as a "shielding" region, the heavily doped p++ region 14 in McCormack can not function as a shielding layer since it only covers a portion of the substrate layer.** In fact, not only does McCormack fail to disclose a "shielding layer," **McCormack actually teaches away from a "shielding layer."** In Column 6, Lines 40-44, McCormack states that "one having ordinary skilled in the art would understand that the heavily doped regions are formed only in areas where P-wells are to be built." (Emphasis added).

As shown above, neither Puar nor McCormack teach or suggest the limitation of "a shielding layer, wherein said shielding layer reduces transfer of noise in the chip," as recited by the Applicant in independent claim 1. For at least the reasons set forth above, the Applicant respectfully asserts that claim 1 is allowable over McCormack and Puar. The Applicant requests that the rejection of claim 1 be withdrawn.

**B. The Examiner's Arguments in the February 14, 2007 Advisory Office Action (AOA) Regarding the Combination of McCormack and Puar**

On pages 2-3 of the AOA, the Examiner states the following (emphasis added):

[A]t column 4, lines 9-13, McCormack states that:

"A conventional way to reduce latchup susceptibility is to lower the resistance of the P-wells. A low P-well resistance has the effect of

decoupling the parasitic bipolar transistors formed by the source/drain regions and the n and p tubs in a CMOS process."

From this statement, one of ordinary skill in the art would recognize that the parasitic bipolar transistors formed by the source/drain regions and the n and p tubs in a CMOS shown in Fig. 2 are **prevented by lower the resistance of the lightly doped (p-) substrate 10. The low resistance lightly doped (p-) substrate 10 is provided by placing higher doped (p) layer 12 on top of the lightly doped (p-) substrate 10.**

The Applicant respectfully disagrees with the above assertions by the Examiner. As seen from the underlined citation above, McCormack discloses that **the conventional way to reduce latchup susceptibility is to lower the resistance of the *P-wells*, not the resistance of the *substrate* as suggested by the Examiner. There is absolutely no mention or suggestion in McCormack that latchup susceptibility may be reduced by lowering the resistance of the substrate "by placing a higher doped layer 12 on top of the lightly doped substrate 10," as alleged by the Examiner.** This is further evidenced by the fact that McCormack's solution for reducing the latchup susceptibility is to use a heavily doped region p++ (14) underneath the p-well (16), and not to reduce the resistance of the substrate 10. The Examiner is simply making conclusory statements without any justification whatsoever.

### C. Rejection of Dependent Claim 2-3

Claims 2-3 depend on independent claim 1. Therefore, the Applicant submits that claims 2-3 are allowable over the references cited in the Final Office Action at least for the reasons stated above with regard to claim 1. The Applicant also reserves the

right to argue additional reasons beyond those set forth above to support the allowability of claims 2-3.

**D. Rejection of Dependent Claim 4**

Claim 4 depends on independent claim 1. Therefore, the Applicant submits that claim 4 is allowable over the references cited in the Final Office Action at least for the reasons stated above with regard to claim 1.

With regard to claim 4, the Final Office Action states the following:

> Regarding claims 2-7, McCormack (Fig. 2) further discloses a transistor 28 of a second transistor type (N type) disposed within the transistor well layer 16 and coupled to the shielding layer 12, wherein the transistor 28 has a transistor well layer 16 of P type is resistivity coupled to the shielding layer 12 of P type and has a first noisy voltage source 24 (column 3, lines 53-55) coupled to a source 17 of the transistor 28.

*See* the Final Office Action at page 4. The Examiner is silent as to Applicant's claim 4. Referring to Figure 2 of McCormack, **McCormack does not disclose or suggest that the "at least one transistor of said second transistor type is disposed within said transistor layer,"** as recited by the Applicant in claim 4.

Therefore, the Applicant submits that claim 4 is allowable over the references cited in the Final Office Action at least for the above reasons. The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claim 4.

**E. Rejection of Dependent Claim 5**

Claim 5 depends on independent claim 1. Therefore, the Applicant submits that claim 5 is allowable over the references cited in the Final Office Action at least for the reasons stated above with regard to claim 1.

With regard to claim 5, the Final Office Action states the following:

> Regarding claims 2-7, McCormack (Fig. 2) further discloses a transistor 28 of a second transistor type (N type) disposed within the transistor well layer 16 and coupled to the shielding layer 12, wherein the transistor 28 has a transistor well layer 16 of P type is resistivity coupled to the shielding layer 12 of P type and has a first noisy voltage source 24 (column 3, lines 53-55) coupled to a source 17 of the transistor 28.

*See* the Final Office Action at page 4. Referring to Figure 2 of McCormack, McCormack does not disclose any resistance that couples the transistor of second transistor type and the shielding layer. Therefore, McCormack does not disclose "said at least one transistor of said second transistor type is resistively coupled to said shielding layer," as recited in Applicant's claim 5.

Therefore, the Applicant submits that claim 5 is allowable over the references cited in the Final Office Action at least for the above reasons. The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claim 5.

**F. Rejection of Dependent Claims 6-7**

Claim 6 depends on independent claim 1. Therefore, the Applicant submits that claim 6 is allowable over the references cited in the Final Office Action at least for the reasons stated above with regard to claim 1.

With regard to claims 6-7, the Final Office Action states the following:

> Regarding claims 2-7, McCormack (Fig. 2) further discloses a transistor 28 of a second transistor type (N type) disposed within the transistor well layer 16 and coupled to the shielding layer 12, wherein the transistor 28 has a transistor well layer 16 of P type is resistivity coupled to the shielding layer 12 of P type and has a first noisy voltage source 24 (column 3, lines 53-55) coupled to a source 17 of the transistor 28.

*See* the Final Office Action at page 4. Referring to Figure 2 of McCormack, **terminal 24 is digital ground - it is not a noisy voltage source**, as erroneously claimed by the Examiner. In fact, terminal 24 is simply a ground terminal and it is not any voltage source. Therefore, McCormack does not disclose "a first noisy voltage source coupled to said at least one transistor of said second transistor type," as recited in Applicant's claim 6.

Therefore, the Applicant submits that claim 6 is allowable over the references cited in the Final Office Action at least for the above reasons. Claim 7 is dependent on claim 6 and is, therefore, allowable at least for the above reasons. The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 6-7.

**G. Rejection of Dependent Claims 8 and 9**

Claims 8-9 depend on independent claim 1. Therefore, the Applicant submits that claims 8-9 are allowable over the references cited in the Final Office Action at least for the reasons stated above with regard to claim 1. The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 8-9.

**H. Rejection of Dependent Claim 10**

Claim 10 depends on independent claim 1. Therefore, the Applicant submits that claim 10 is allowable over the references cited in the Final Office Action at least for the reasons stated above with regard to claim 1.

With regard to claim 10, the Final Office Action states the following:

> Regarding claim 10, McCormack (Fig. 2) further discloses that the transistor 30 has a transistor well layer 22 of N type is capacitively coupled to the shielding layer 12 of P type.

*See* the Final Office Action at page 4. Referring to Figure 2 of McCormack, the Applicant points out that there is no capacitor coupling the transistor of first transistor type to the shielding layer. Therefore, McCormack does not disclose or suggest "wherein said at least one transistor of said first transistor type is capacitively coupled to said shielding layer," as recited in Applicant's claim 10.

Therefore, the Applicant submits that claim 10 is allowable over the references cited in the Final Office Action at least for the reasons stated above. The Applicant also

reserves the right to argue additional reasons beyond those set forth above to support the allowability of claim 10.

**I. Rejection of Dependent Claim 12**

Claim 12 depends on independent claim 1. Therefore, the Applicant submits that claims 8-9 are allowable over the references cited in the Final Office Action at least for the reasons stated above with regard to claim 1. The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claim 12.

**J. Rejection of Dependent Claim 14 and 15**

Claims 14 and 15 depend on independent claim 1. Therefore, the Applicant submits that claims 14 and 15 are allowable over the references cited in the Final Office Action at least for the reasons stated above with regard to claim 1.

With regard to claims 14 and 15, the Final Office Action states the following at page 3:

> Puar (Fig. 5) further discloses a noisy voltage source 38 of positive (column 4, lines 59-63) coupled to a source of the transistor.

Puar, at the above citation discloses the following:

> To avoid this problem, the analog circuits according to the present invention are designed with mostly P-channel transistors within

> independent N-wells which are connected to the positive and relatively quiet-reference voltage, VDD, as shown in **FIG.** 5.

*See* Puar, col. 4, lines 59-63. As it can be clearly noted from the citation, Puar does not disclose or suggest "a noisy voltage source coupled to said at least one transistor of a first transistor type," as recited in Applicant's claims 14-15. Accordingly, the Applicant submits that claims 14 and 15 are allowable over the references cited in the Final Office Action at least for the above reasons. The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 14 and 15.

## II. The Proposed Combination of McCormack, Puar and Wei Does Not Render Claims 11 and 13 Unpatentable

Claims 11 and 13 depend from independent claim 1. Since Puar and Wei do not cure the deficiencies of McCormack, the Applicant submits that claims 11 and 13 are allowable at least for the reasons stated above with regard to allowability of claim 1.

The Examiner states the following in the Final Office Action:

> McCormack discloses the shielding layer 12 is deep P-well, but not N-well which is capacitively coupled to the substrate layer 10. However, Wei teaches the conventional of forming a transistor within a shielding layer of P-well, which is capacitively coupled to the N type substrate (Fig. 3), or a transistor within a shielding layer of N-well, which is capacitively coupled to the P type substrate (Fig. 4). Accordingly, it would have been obvious to form the shielding layer 12 of McCormack with either N type or P type because they both provide the benefits of eliminating substrate effect , as taught by Wei (column 1 ; lines 47-60).

*See* the Final Office Action at pages 4-5. The Applicant respectfully disagrees and points out that **none of the referenced cases (McCormack, Puar or Wei), including the above citation by the Examiner of Fig. 4 of Wei, disclose a capacitive coupling (i.e., via a capacitor) between a shielding layer and a substrate layer. Furthermore, none of the referenced cases disclose a shielding layer comprising of deep N-well.** Therefore, the combination of Puar-Wei-McCormack does not disclose "said shielding layer is capacitively coupled to said substrate layer," as recited by Applicant's claim 11, and "said shielding layer is a deep N-well," as recited by Applicant's claim 13.

The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 11 and 13.

## III. The Proposed Combination of Wei and Puar Does Not Render Claims 1-13 Unpatentable

The Applicant now turns to the rejection of claims 1-13 as being unpatentable over Wei in view of Puar.

### A. Rejection of Claim 1

With regard to the rejection of independent claim 1 under 103(a), the Applicant submits that the combination of Wei and Puar does not disclose or suggest at least the limitation of "at least one transistor of a first transistor type that couples said transistor

layer to said shielding layer," as recited by the Applicant in independent claim 1. The Final Office Action states:

> Wei (Fig . 4) discloses a system for reducing noise in a chip, the system comprising: a substrate layer integrated within the chip; a transistor layer 46 integrated within the chip, which is shielded from the substrate layer by a shielding layer N-well 484, wherein the shielding layer N-well 484 reduces the transfer of noise or body effect in the chip (column 1, lines 55-60); **a transistor G4 of a first transistor type (p type) that couples the transistor layer 46 to the shielding layer 484**; and a positive potential Vcc (+5V) of a voltage source coupled to the transistor G4. (emphasis added)

*See* the Final Office Action at page 5. With regard to the above bolded portion of the Examiner's argument, the Applicant points out that item G4 designates a ground terminal for the PMOS transistor that is next to the NMOS transistor 46 (note that the PMOS transistor of Wei is not numbered in Figure 4, but it is numbered 52 in Figure 5). In this regard, G4 of Wei does not designate a "transistor". Furthermore, as illustrated in Figure 4 of Wei, Wei does not disclose or suggest any transistor that couples a transistor layer of any of the PMOS or NMOS 46 with the alleged shielding layer 484. Therefore, the Applicant submits that the combination of Wei and Puar does not disclose or suggest at least the limitation of "at least one transistor of a first transistor type that couples said transistor layer to said shielding layer," as recited by the Applicant in independent claim 1. Accordingly, the proposed combination of Wei and Puar does not render independent claim 1 unpatentable, and a *prima facie* case of obviousness has not been established. The Applicant submits that claim 1 is allowable at least for the above reasons.

**B. Rejection of Dependent Claims 8 and 13**

Based on at least the foregoing, the Applicant believes the rejection of independent claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Wei in view of Puar has been overcome and requests that the rejection be withdrawn. Additionally, claims 8 and 13 depend from independent claim 1, respectively, and are, consequently, also respectfully submitted to be allowable at least for the above reasons.

The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 8 and 13.

**C. Rejection of Dependent Claims 2-7**

Claims 2-7 depend on independent claim 1. Therefore, the Applicant submits that claims 2-7 are allowable over the references cited in the Final Office Action at least for the reasons stated above with regard to claim 1.

With regard to claims 2-7, the Final Office Action states the following:

> Regarding claims 2-7, Wei (Fig. 4) further discloses: a second transistor G3 of Ntype disposed within the transistor layer 46 and resistivity coupled to the N-well shielding layer 484; and a first noisy voltage source GND (0V) coupled to a source S3 of the second transistor type G3.

*See* the Final Office Action at page 6. The Applicant respectfully disagrees. Referring to Figure 4 of Wei, **G3 is a ground terminal and not a transistor**. Furthermore, **Wei does not disclose a transistor of a second transistor type that is resistively**

**coupled (i.e., via a resistance) to the shielding layer. In addition, Wei discloses a ground terminal (GND), which is not a voltage source.** Wei also does not disclose that GND is a noisy voltage source, as recited in Applicant's claim 7, for example.

Therefore, the Applicant submits that claims 2-7 are allowable over the references cited in the Final Office Action at least for the reasons stated above. The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 2-7.

**D. Rejection of Dependent Claims 9-12**

Claims 9-12 depend on independent claim 1. Therefore, the Applicant submits that claims 9-12 are allowable over the references cited in the Final Office Action at least for the reasons stated above with regard to claim 1.

With regard to claims 9-12, the Final Office Action states the following:

> Regarding claims 9-10 and 11 -12, Wei (Fig. 4) also discloses: the first transistor G4 of P-type disposed within the transistor layer 46 and capacitively coupled to the N-well shielding layer 484; and the N-well shielding layer 484 capacitively coupled to the P-type substrate layer and disposed between the substrate layer and the transistor layer 46.

*See* the Final Office Action at page 6. The Applicant respectfully disagrees. Referring to Figure 4 of Wei, **G4 is a ground terminal and not a transistor**. Furthermore, **Wei does not disclose a transistor of a first transistor type that is capacitively coupled (i.e., via a capacitor) to the shielding layer.**

Therefore, the Applicant submits that claims 9-12 are allowable over the references cited in the Final Office Action at least for the reasons stated above. The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 9-12.

## CONCLUSION

For at least the foregoing reasons, the Applicant submits that claims 1-15 are in condition for allowance. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge $500 (to cover the Brief on Appeal Fee) and any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Respectfully submitted,

Date: 27-APR-2007

By: _____
Ognyan Beremski, Reg. No. 51,458
Attorney for Applicant

McANDREWS, HELD & MALLOY, LTD.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
Telephone: (312) 775-8000
Facsimile: (312) 775 – 8100

(OIB)

## CLAIMS APPENDIX
## (37 C.F.R. § 41.37(c)(1)(viii))

1. A system for reducing noise in a chip, the system comprising:

a substrate layer integrated within the chip;

a transistor layer integrated within the chip, which is shielded from said substrate layer by a shielding layer, wherein said shielding layer reduces transfer of noise in the chip;

at least one transistor of a first transistor type that couples said transistor layer to said shielding layer; and

a positive potential of a quiet voltage source that is coupled to said at least one transistor of said first transistor type.

2. The system according to claim 1, comprising at least one transistor of a second transistor type coupled to said shielding layer.

3. The system according to claim 2, wherein said at least one transistor of said second transistor type is an n-type transistor.

4. The system according to claim 2, wherein said at least one transistor of said second transistor type is disposed within said transistor layer.

5. The system according to claim 2, wherein said at least one transistor of said second transistor type is resistively coupled to said shielding layer.

6. The system according to claim 2, comprising a first noisy voltage source coupled to said at least one transistor of said second transistor type.

7. The system according to claim 6, wherein said first noisy voltage source is coupled to a source of said at least one transistor of said second transistor type.

8. The system according to claim 1, wherein said at least one transistor of said first transistor type is a p-type.

9. The system according to claim 1, wherein said at least one transistor of said first transistor type is disposed within said transistor layer.

10. The system according to claim 1, wherein said at least one transistor of said first transistor type is capacitively coupled to said shielding layer.

11. The system according to claim 1, wherein said shielding layer is capacitively coupled to said substrate layer.

12. The system according to claim 1, wherein said shielding layer is disposed between said substrate layer and said transistor layer.

13. The system according to claim 1, wherein said shielding layer is a deep N-well.

14. The system according to claim 1, comprising a noisy voltage source coupled to said at least one transistor of a first transistor type.

15. The system according to claim 14, wherein said noisy voltage source is coupled to a source of said at least one transistor of a first transistor type.

## EVIDENCE APPENDIX
## (37 C.F.R. § 41.37(c)(1)(ix))

(1) United States Patent No. 6,395,591 ("McCormack"), entered into record by the Examiner in the August 11, 2004 Office Action.

(2) United States Patent No. 6,356,497 ("Puar"), entered into record by the Examiner in the August 11, 2004 Office Action.

(3) United States Patent No. 6,403,992 ("Wei"), entered into record by the Examiner in the August 11, 2004 Office Action.

## RELATED PROCEEDINGS APPENDIX
## (37 C.F.R. § 41.37(c)(1)(x))

The Appellant is unaware of any related appeals or interferences.